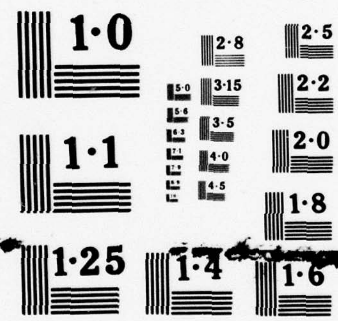
AD-A055 950 MICROWAVE ASSOCIATES INC BURLINGTON MASS F/G 9/1
MM AND T PROGRAM FOR THE ESTABLISHMENT OF PRODUCTION TECHNIQUES--ETC(U)
OCT 77 Y ANAND, R BILOTTA DAAB07-76-C-0039

UNCLASSIFIED ECOM-0039-5 NL

1 OF 1
ADA
055950

END
DATE
FILMED
8-78
DDC

END
DATE
FILMED
8-78
DDC



NATIONAL BUREAU OF STANDARDS
MICROCOPY RESOLUTION TEST CHART

FOR FURTHER TRAN

4049 088

12

AD

AD A055950

AD No.____
DDC FILE COPY

Research and Development Technical Report
ECOM - 0039 - 5

MM&T Program for the Establishment of Production Techniques for High Power Bulk Semiconductor Limiters

5TH QUARTERLY REPORT

By

Y. ANAND R. BILOTTA

OCTOBER 1977

DISTRIBUTION STATEMENT
Approved for public release; distribution unlimited.

Monitored by:

ECOM
US ARMY ELECTRONICS COMMAND • FORT MONMOUTH, NEW JERSEY 07703

CONTRACT DAAB07-76-C-0039
MICROWAVE ASSOCIATES, INC.
Burlington, Massachusetts 01803

Disclaimers

The findings in this report are not to be construed as an Official Department of the Army position, unless so designated by other authorized documents.

The citation of trade names and names of manufacturers in this report is not to be construed as official Government indorsement or approval of commercial products of services referenced herein.

Disposition

Destroy this report when it is no longer needed. Do not return it to the originator.

TR ECOM-0039-5
October 1977

REPORTS CONTROL SYMBOL
OSD-1366

MM&T PROGRAM FOR THE ESTABLISHMENT OF PRODUCTION TECHNIQUES FOR HIGH POWER BULK SEMICONDUCTOR LIMITERS

FIFTH QUARTERLY REPORT

23 June 1977 to 22 September 1977

Distribution Statement

Distribution unlimited: Approved for public release

Prepared By

Dr. Y. Anand

R. Bilotta

MICROWAVE ASSOCIATES, INC.
BURLINGTON, MASSACHUSETTS 01803

FOR

U.S. ARMY ELECTRONICS COMMAND, FORT MONMOUTH, NJ 07703

19 REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

18 1. REPORT NUMBER: ECOM 0039-5 and

2. GOVT ACCESSION NO.

3. RECIPIENT'S CATALOG NUMBER: 9

6 4. TITLE (and Subtitle): MMT Program for the Establishment of Production Techniques for High Power Bulk Semiconductor Limiters.

5. TYPE OF REPORT & PERIOD COVERED: [redacted] Quarterly rept. no. 5, 23 Jun [redacted] - 22 Sep [redacted] 77

6. PERFORMING ORG. REPORT NUMBER

10 7. AUTHOR(s): [redacted] Yoginder Anand, [redacted] Richard Bilotta

8. CONTRACT OR GRANT NUMBER(s): 15 DAAB07-76-C-0039

9. PERFORMING ORGANIZATION NAME AND ADDRESS: Microwave Associates, Inc., Burlington, MA 01803

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 2769771

11. CONTROLLING OFFICE NAME AND ADDRESS: U.S. Army Electronics Command, Fort Monmouth, NJ 07703

12. REPORT DATE: 11 Oct [redacted] 77

13. NUMBER OF PAGES: 38 12 36p.

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)

15. SECURITY CLASS. (of this report): UNCLASSIFIED

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Limiters
Bulk Effect
Silicon Processing
Switches

RHO

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

X-band bulk limiters of 3.5 mils in thickness have been fabricated using high resistivity silicon ρ = 12,000 to 18,000 ohm-cm, P-type uncompensated <111> orientation. These bulk limiters exhibit 3 dB bandwidth of 0.6 to 0.8 GHz and power handling capability of 20 - 30 kW.

As a cost reduction measure, low cost stamped X-band copper irises have been introduced for mounting the bulk limiter chips. This would

229400

CL

substantially lower the price of bulk limiter assembly. Various parameters are being optimized to achieve both bandwidth and RF power goals of the contract.

TABLE OF CONTENTS

LIST OF TABLES

ABSTRACT

X-band bulk limiters of 3.5 mils in thickness have been fabricated using high resistivity silicon $\rho = 12{,}000$ to 18,000 ohm-cm, P-type uncompensated <111> orientation. These bulk limiters exhibit 3 dB bandwidth of 0.6 to 0.8 GHz and power handling capability of 20 - 30 kW.

As a cost reduction measure, low cost stamped X-band copper irises have been introduced for mounting the bulk limiter chips. This would substantially lower the price of bulk limiter assembly. Various parameters are being optimized to achieve both bandwidth and RF power goals of the contract.

A-049-058

PURPOSE

The objective of this program is to establish a production capability to manufacture High Power Bulk Semiconductor Limiters per U.S. Army Electronics Command Technical Requirements SCS-486.

The specification covers X-band high power bulk semiconductor limiter and low power multistage clean-up limiter. Four fundamental requirements are detailed in the specifications. They are, (1) recovery time, (2) high power capability, (3) insertion loss, and (4) VSWR.

A total of fifteen (15) engineering sample limiters, twenty (20) confirmatory sample limiters and fifty (50) pilot run production limiters will be supplied. A pilot line capable of producing 100 bulk semiconductor limiters per month will be demonstrated. Reports and documentation as required in Sections E, F, G and H of DAAB07-76-Q-0040 and as detailed in Section 3.5 of ECIPPR No. 15, dated December 1976, will be provided.

The program divides into the following four phases, Phase I - Engineering Samples (300 days), Phase II - Confirmatory Sample Production (240 days), Phase III - Pilot Line Production (180 days), and Phase IV - Final Documentation (30 days). The total program duration is 750 days.

During Phase I of this program, a number of factors in fabricating bulk semiconductor limiters are being investigated. These include iris formation, circuit configuration, material characterization and chip mounting. Efforts during Phase I will be directed toward selecting a single limiter design capable of meeting the objectives of SCS-486.

The optimum device design will be chosen at the end of Phase I. In Phases II, III and IV, a single device design will be produced.

The major effort of this program will be realization of a single bulk limiter design which meets all the objectives of SCS-486. Individually, any of the goals described can be currently obtained. Recognizably, it is the development of a single component design which achieves all of the desired performance parameters that is the formidable engineering and manufacturing endeavor.

I. OBJECTIVE

The objective of the current Manufacturing Methods and Technology Engineering program is to establish the producibility of the X-band bulk semiconductor limiter and the X-band bulk semiconductor lower power diode multistage limiter by mass production techniques. Achieving the performance goals of the program represents a formidable engineering task. These goals, from SCS-486, are summarized below.

A. Function Description

The high power, solid state, limiter described herein will operate in the frequency band 9.0 - 9.65 GHz. A multi-stage configuration is acceptable with the first stage incorporating the principle of avalanche breakdown of near-intrinsic silicon to achieve isolation. This device will be mounted in a fixed tuned resonant waveguide cavity designed to provide the necessary avalanche field conditions. The second stage shall be either a bulk effect device or a common semiconductor diode limiter. Both limiter devices will be mounted in a common structure and no external bias or drive will be necessary for its operation. The receiver protector is required to operate in unpressurized conditions.

B. Mechanical Characteristics

The bulk semiconductor limiter structure will have the following performance objectives:

Weight	:	7.0 oz maximum
Input Flange	:	mates with UG-40B/U choke flange
Output Flange	:	mates with UG-135/U cover flange
Mounting Position	:	any
Cooling	:	conduction

C. Electrical Characteristics

The bulk semiconductor limiter will have the following objectives:

Peak RF Input Power	: 30 kW, Du = 0.001
1 μsec Pulses Continuous	: 10 kW, Du = 0.01
Insertion Loss	: 0.7 dB (maximum)
Low Level VSWR	: 1.4:1 (maximum)
Recovery Time	: 0.8 μsec (maximum)
Flat Leakage	: 50 mW (max), for 30 kW, .001 duty cycle, 1 μsec pulse
Spike Leakage	: 750 mW (max), for 30 kW, .001 duty cycle, 1 μsec pulse
External Bias	: none

D. Absolute Rating Objectives

PARAMETER	SYMBOL	MIN	MAX	UNIT
Frequency	F	9.0	9.65	GHz
Peak Power	P	--	30	kW
Average Power	P_a	--	100	W
Ambient Temp.	T_A	-55	+85	^oC
Altitude	--	--	50,000	ft

II. INTRODUCTION

This report covers the period from 23 June through 22 September 1977. During this period, semiconductor limiter work was concentrated in the areas of semiconductor wafer processing, device fabrication and bulk limiter circuit analysis.

Significant improvements in the semiconductor procedures have been accomplished during the quarter. A low cost "stamped" X-band copper irises have been introduced for mounting bulk limiter chips. The cost of a stamped iris is 20 cents compared to $15.00 of a machined iris; this would substantially lower the price of bulk limiter assembly.

Theoretical investigation was carried out to improve the low level RF performance of the bulk and clean-up limiters. The computer model chosen was a simple filter structure consisting to two lumped capacitances and a lumped inductance. In this model, the lumped capacitances were represented by bulk limiters and the lumped inductance physically by an inductive iris. Optimized parameters have been obtained and physical realization of this circuit and experimentation were conducted during the quarter.

The subsequent sections of this report describe in great detail the work performed and results achieved to date.

III. BULK SEMICONDUCTOR CIRCUIT TUNING ANALYSIS

During this quarter, an attempt was made to physically realize the tuning circuit described in the Fourth Quarterly Report.

A model of a simple filter structure was described consisting of two lumped capacitances and a lumped inductance. The capacitances represent bulk limiters and the lumped inductance can be realized by an inductive iris (see Figure 1).

The model was analyzed with a computer program developed by Microwave Associates which allows to solve for steady-state characteristics of microwave networks composed of transmission lines and networks of capacitors, inductors and resistors. The results of this analysis are given in Tables I and II.

Unfortunately, physical realization of the circuit was unsuccessful. Extensive testing was done with various types of iris - bulk limiter combinations to no avail. The experiment was unsuccessful because the computer model did not take into account the fringing effects which occur when placing the reactive elements so close together.

In conclusion, it would seem that this technique, although a worthwhile exercise, was unsuccessful. To date, the best tuning structure developed is that of the First Engineering Sample in which lumped capacitances are used to transform into and out of the bulk limiter.

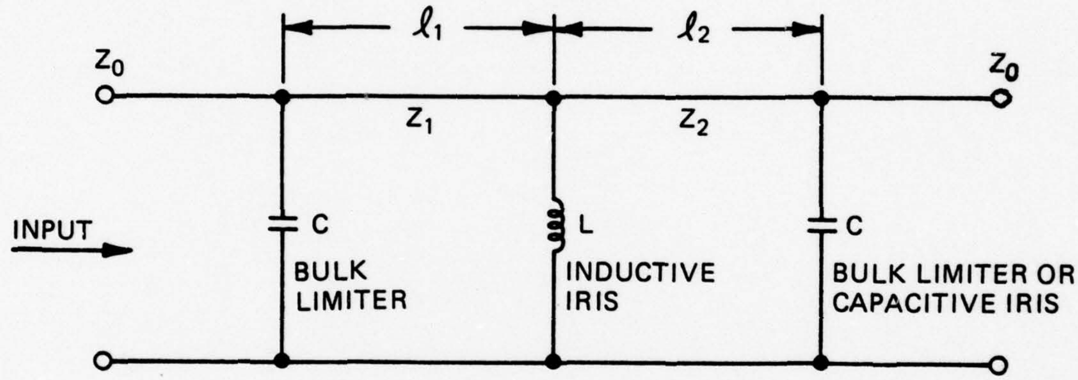


FIGURE 1 CIRCUIT MODEL

FREQUENCY	VSWR	LOSS
8.50	2.942	1.208
8.60	2.246	0.692
8.70	1.760	0.342
8.80	1.426	0.136
8.90	1.201	0.036
9.00	1.054	0.003
9.10	1.037	0.001
9.20	1.086	0.007
9.30	1.091	0.008
9.40	1.050	0.003
9.50	1.032	0.001
9.60	1.166	0.026
9.70	1.374	0.109
9.80	1.682	0.290
9.90	2.132	0.608
10.00	2.779	1.088

TABLE I. Computer Print Out of Circuit Model

PARAMETER	VALUE
C	0.25 picofarads
L	0.18 nanohenries
Z_0	471 ohms
Z_1	515 ohms
Z_2	515 ohms
ℓ_1	0.032 inches
ℓ_2	0.032 inches

TABLE II. Final Circuit Values for the Optimized Model

IV. FABRICATION AND RF TEST RESULTS

During the last quarter, eight (8) high resistivity wafers (ρ = 12,000 to 18,000 ohm-cm, < 111 >, P-type uncompensated) from Wacker Chemical and were processed for bulk limiters. These wafers were etched and polished to 3.5 mils in thickness. The phosphorous and boron diffusions were done on both sides of the wafers at 1000^oC and 950^oC, respectively. The 3/4 mil square checkerboard pattern was used prior to the boron diffusion. Boron nitride source was used as the dopant source during the boron diffusion. Both surfaces of a wafer were then metallized with 500 - 1000 Å layer of titanium (10%) and tungsten (90%) alloy and 2000 - 3000 Å layer of gold and then electroplated with pure gold. Both the surfaces were plated to a thickness of 3.0 mils. The active elements area were defined by etching 10 mils in diameter gold posts on the top side of the wafer. The posts were etched to a height of 3 mils using conventional photolithographic and photoresist flow techniques. The silicon mesa etching process was performed when the elements were still in wafer form. Then the wafer was cut into 40 mil squares and were separated into individual chips. The gold posts of the bulk limiter chips were ball bonded to gold wire (5 mil in diameter). These chips were passivated with silicon nitride and Dow Corning DC-643 Junction Coating. The bulk limiter chips were mounted in low cost "stamped" gold plated copper X-band irises and were tested for both low and high level RF performance.

A. Evaluation of Stamped Irises

X-band irises were stamped commercially from 0.062 inch thick oxygen-free high conductivity copper. The burrs were removed from the irises by filing and sanding operations. The irises were cleaned thoroughly and then nickel and gold were electroplated. Bulk limiter chips

from BL-26A run were mounted in these irises and were tested for both low level and high level RF performance. Results are given in Tables III and IV and shows that these bulk limiters exhibit low insertion loss and low recovery time and are capable of handling 20 kW RF power.

The above results also show that stamped irises performed very well and can replace machined irises. The cost of a stamped iris is 20 cents compared to $15.00 of a machined iris. This would substantially lower the price of bulk limiter assembly.

			UNTUNED		TUNED FOR PACKAGE		
Iris Number	Resistance (ohm)	Capacitance (pF)	F_o (GHz)	Li at F_o (dB)	F_o (GHz)	Li at F_o (dB)	3 dB Bandwidth (GHz)
BL-26-1	150	0.15	10.46	1.0	9.3	0.7	.700
BL-26-2	175	0.14	10.8	0.8	9.3	0.6	.600
BL-26-3	150	0.17	10.2	0.7	9.3	0.7	.700
BL-26-4	200	0.16	10.5	0.8	9.3	0.8	.800
BL-26-5	175	0.14	11.0	0.9	9.3	0.6	.700

TABLE III. DC and RF Characteristics of Bulk Limiters using Low Cost "Stamped" Irises (3.5 mil thick wafer and TiW - Au metallization)

Bulk Limiter Number	F_o (GHz)	Pulse Length (μsec)	Repetition Rate (Hz)	Peak Power (kW)	Recovery Time (μsec)
BL-26-1	9.3	0.25	4000	25	2.0
BL-26-2	9.3	0.25	4000	30	2.0
BL-26-3	9.3	0.25	4000	28	2.0
BL-26-4	9.3	0.25	4000	20	2.0
BL-26-5	9.3	0.25	4000	24	2.0

TABLE IV. High Power RF Characteristics of Bulk Limiters using Low Cost "Stamped" Irises

V. PROBLEM AREAS

A. Recovery Time

The recovery times obtained with both single and dual slot bulk limiters have been in the order of 1.5 to 2 microseconds. This may be reduced by geometry changes being incorporated in the batch fabrication work currently underway.

VI. CONCLUSIONS

X-band bulk limiters have been fabricated using high resistivity silicon with ρ = 12,000 to 18,000 ohm-cm, P-type, uncompensated <111> orientation from Wacker Chemical Company. These bulk limiters exhibit 3 dB bandwidth of 0.6 to 0.8 GHz and power handling capability of 20 - 30 kW. Low cost stamped irises have been introduced for mounting the bulk limiter chips. The stamped irises performed very well and can replace high price machined irises.

VII. PROGRAM FOR THE NEXT QUARTER

During the next quarter, we will fabricate devices using low cost stamped irises. Batch process and ball bonding techniques will be optimized to improve the yield of good quality bulk limiters. Confirmatory sample units will be fabricated and shipped on schedule.

VIII. IDENTIFICATION OF PERSONNEL

During this quarter, the following technical personnel contributed to this program.

Title	Manhours
Project Manager	100
Silicon Materials Manager	10
Senior Processing Engineer	30
Processing Engineer	40
Limiter Engineer	50
Engineering Assistant (Fabrication)	200
Engineering Assistant (Test)	300

Electronic Command
Technical Requirements

SCS-486
28 March 1975

High Power Bulk Semiconductor Limiter

1. SCOPE: This specification describes a passive, solid state, receiver protector using a bulk semiconductor limiter in combination with a semiconductor diode limiter. Limiter operation will provide isolation from x-Band pulses up to 30 kw over a variety of test conditions.

2. APPLICABLE DOCUMENTS

2.1 Documents. - The following documents, of issue in effect on the date of invitation for bids, form a part of this specification to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-E-1	General Specification for Electron Tube
MIL-P-11268	Parts, Materials, and Processes Used in Electronic Equipment

STANDARDS

MILITARY

MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes
MIL-STD-202	Test Methods for Electronic and Electrical Components Parts
MIL-STD-1311A	Microwave Oscillator Test Methods

(Copies of specifications, standards and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer. Both the title and number of symbol should be stipulated when requesting copies.)

FSC 5961

REQUIREMENTS:

3.1 Function Description. - The high power, solid state, limiter specified herein will operate in the frequency band 9.0 - 9.65 GHZ. A multi-stage configuration is acceptable with the first stage incorporating the principle of avalanche breakdown of near-intrinsic silicon to achieve isolation. This device will be mounted in a fixed turned resonant waveguide cavity designed to provide the necessary avalanche field conditions. The second stage shall be either a bulk effect device or a semiconductor diode limiter. Both limiter devices will be mounted in a common structure and no external bias or drive will be necessary for its operation. The receiver protector is required to operate in unpressurized conditions.

3.2 Mechanical Characteristics. - The bulk semiconductor limiter structure will conform to the following requirements:

(a)	Weight	20 oz max
(b)	Input flange	mates with UG-40B/U choke flange
(c)	Output flange	mates with UG-135/U cover flange
(d)	Mounting position	any
(e)	Cooling	conduction

3.2.1 Physical Dimensions. - The bulk semiconductor limiter shall conform to Figure 1.

3.2.2 Construction. - Parts and materials will be in accordance with MIL-P-11268.

3.3 Electrical characteristics. - The bulk semiconductor limiter will conform to the following requirements:

(a)	Peak Rf Input power, 1 μsec pulses continuous :	30 kw, Du = .001 10 kw, Du = .01
(b)	Insertion Loss :	0.7dB (max)
(c)	Low Level VSWR :	1.4:1 (max)
(d)	Recovery Time :	0.8 μsec (max)
(e)	Flat Leakage :	50 mw (max), for 30 kw, .001 duty cycle, 1 μsec pulse
(f)	Spike Leakage :	750 mw (max), for 30 kw, .001 duty cycle, 1 μsec pulse
(g)	external bias :	none

3.4 Absolute Ratings

Parameter	Symbol	Min	Max	Unit
Frequency	F	9.0	9.65	GHZ
Peak Power	P		30	kw
Average Power	Pa		100	w
Ambient Temp.	T_A	-55	+85	°C
Altitude	—		50,000	ft

3.5 Marking. - Each bulk semiconductor limiter shall be marked with the following information:

(a) Manufacturer's model number

(b) Manufacturer's serial number, individually for each limiter.

(c) rf input port.

(d) rf output port.

4. QUALITY ASSURANCE PROVISIONS

4.1 Inspection.

4.1.1 Responsibility for inspection. - The contractor is responsible for the performance of all inspection requirements as specified herein. The contractor may utilize his own facilities or any commercial laboratory acceptable to the government. The government reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements. Inspection records of the examinations and tests shall be kept complete and available to the government.

4.1.2 Test equipment c inspection facilities. - Test equi, ent and inspection facilities shall be of sufficient accuracy, quality, and quantity to permit performance of the required inspection. The supplier shall establish calibration of inspection equipment to the satisfaction of the government.

4.2 Classification of inspection. - The examination and testing of limiters shall be classified as follows:

a. First article inspection (see 4.3).

b. Quality conformance inspection (see 4.4.).

G-1
4.3 First article inspection. - First article inspection shall be performed by the supplier, after award of contract and prior to production at a location acceptable to the government. It shall be performed on sample units which have been produced with equipment and procedures which will be used in production. This inspection shall consist of QCI-1, QCI-2 and QCI-3 inspection in accordance with 4.4.1, 4.4.2 and 4.4.3.

4.3.1 Sample. - Twenty (20) limiters shall be submitted for first article inspection.

P.2A
4.4 Quality Conformance Inspection.

4.4.1 Quality conformance inspection - Part 1 (QCI-1). - Every limiter shall be tested in all positions of the Quality Conformance Inspection - Part 1 (QCI-1). No failures shall be permitted.

4.4.2 Quality conformance inspection - Part 2 (QCI-2). - The Quality Conformance Inspection - Part 2 (QCI-2) shall be performed in accordance with MIL-STD-105, Inspection Level S1 with an AQL of 6.5%. In the event of lot rejection, tightened inspection procedures shall be invoked. Normal inspection shall be resumed when two (2) consecutive lots have conformed with QCI-2 tests. If the lot size is less than 50 limiters, the sample size shall be one (1) with an acceptance number of zero (0). For purposes of inspection, the lot size shall be one (1) month's production.

4.4.3 Quality conformance inspection - Part 3 (QCI-3). - Three limiters shall undergo continuous life testing for a min. of 2500 hrs. No failures shall be permitted.

4.5 Detailed listings of quality conformance inspection tests. - Quality conformance inspection tests shall be conducted in accordance with Table I (QCI-1), Table II (QCI-2), and Table III (QCI-3).

4.6 Test Conditions

F[illegible]meter Unit	T_A °C	Fo GHZ	Po Watts	μ sec	P_{RR} Pulses/sec	Du	Watts
TC 1	25±3	9.0, 9.375, 9.65±.01	30,000 ± 500	1.0±0.1	1000±25	.001	30
TC 2	25±3	9.0 – 9.65 ± .01	0.001	CW	—	—	—
TC 3	25±3	9.0, 9.375, 9.65±.01	—	1.0±0.1	1000±25	.001	—
TC 4	25±3	9.0, 9.375, 9.65±.01	10,000 ± 250	1.0±0.1	10,000 ±150	.01	100
TC 5	25±3	9.375±.01	30,000 ± 500	1.±0.1	1000 ±25	.001	30
TC 6	—	—	0	—	—	—	—
TC 7	25±3	—	0	—	—	—	—

	Mil Standard	Application Method	Test Condition	Symbol	Limits Lower	Limits Upper	Units	Notes
Maximum Leakage (flat)	1311A	4452A	TC 1	P_f		50	mw	1,3
Maximum Leakage (spike)	1311A	4452A	TC 1	P_s		750	mw	2,3
Insertion Loss	1311A	4416	TC 2	Li		0.7	db	3,4
Low Level VSWR	1311A	4473	TC 2	σ		1.4:1	—	3,4,5
Recovery Time	1311A	4471B (Method B)	TC 1	τ		0.8	μsec	3,8
Firing Power	1311A	4496	TC 3	P_{FR}		150	mw	3,6,8

Quality Conformence Inspection - Part 1 (Qc1-1)

Table II

	Mil Standard	Application Method	Test Condition	Symbol	Lower	Upper	Unit	No.
Maximum Leakage (flat)	1311A	4452A	TC 1	P_f	—	100	W	1,7
Maximum Leakage (spike)	1311A	4452A	TC 1	P_s	—	400	W	2,7
Maximum Leakage (flat)	1311A	4452A	TC 4	P_f	—	50	mw	1,3
Maximum Leakage (spike)	1311A	4452A	TC 4	P_s	—	750	mw	2,3
Recovery Characteristic(phase)	—	—	TC 5	ΔR_p	—	0.5	degree	3,8,9
Recovery Characteristic (amplitude)	—	—	TC 5	ΔR_a	—	0.1	db	3,8,9
Temperature Cycling(non-oper.)	1131A	1027	TC 6	ΔL_i Δf_3 $\Delta \tau$	—	0.2 100 0.2	db mw μ sec	10
Vibration	202E	204C Method A	TC 7	ΔL_i Δf_3 $\Delta \tau$	—	0.2 100 0.2	db mw μ sec	10
Shock	202E	213B Method G	TC 7	ΔL_i Δf_3 $\Delta \tau$	—	0.2 100 0.2	db mw μ sec	10
Humitity	1311A	1011	TC 6	ΔL_i Δf_3 $\Delta \tau$	—	0 0 0	db mw μ sec	10

	Mil Standard	Application Method	Test Condition	Symbol	Limits Lower	Limits Upper	Unit	Notes
Life Test	1311A	4551A	TC 5	t	2500		hours	11
Life Test End-Point (1)	1311A	4452A	TC 1	P_s		1.0	watt	2,3
Life Test End-Point (2)	1311A	4416	TC 2	L_i		0.9	db	3,4
Life Test End-Point (3)	1311A	4471B	TC 1	τ		1.0	μ sec	3
Life Test End-Point (4)	1311A	4452A	TC 1	P_f		75	mw	1,3
Life Test End-Point (5)	1311A	4496	—	P_{FR}		170	mw	3,6

Quality Conformance Inspection - Part 2 (QC111-3)

TES:

The maximum flat leakage shall not exceed the specified limits for test frequencies 9 000, 9.375, .9.650GHZ. The incident Rf pulse will have a risetime 50 nanoseconds maximum. Test configuration reference figure 4452 - 1b. The peak power measurement will be accomplished by calibrating the deflection of a sampling oscilloscope as described in section 3.2 paragraphs 3.2.1 and 3.2.2 of Mil-Std-1311A.

The maximum spike leakage shall not exceed the specified limits for test frequencies 9.000, 9.375, 9.650 GHZ. Oscilloscope calibration technique as described in section 3.2 paragraphs 3.2.1 and 3.2.2 of Mil-Std-1311A is applicable. Amplitude variation shall be recorded by observing the distribution of spike amplitudes for 1 minute time through open shutter of scope camera.

Quality conformance test to be made using multi-stage limiter. For example using the high power bulk stage followed by the limiter diode.

A swept frequency may be used.

Match Termination used in this test circuit shall have a VSWR of 1.05 or less.

The firming power shall be defined as a db increase of limiter insertion loss compared to the "cold" insertion loss.

Quality conformance test to be made using bulk semiconductor stage only.

For this specification the following abbreviations and symbols in addition to MIL-E-1 abbreviations and symbols shall apply; τ = time (recovery), ΔR_p = variation of phase on recovery (total deviation at a fired time), ΔR_a = variation of amplitude on recovery (total deviation at a fixed time), P_{FR} = firing power.

The maximum variation in phase and amplitude as measured by dynamic phase and amplitude test facility shall not vary more than the specified limits over a 1 minute integration time period. Measurement to be made at a point 5 μsec from the cessation of 1 μsec input pulse.

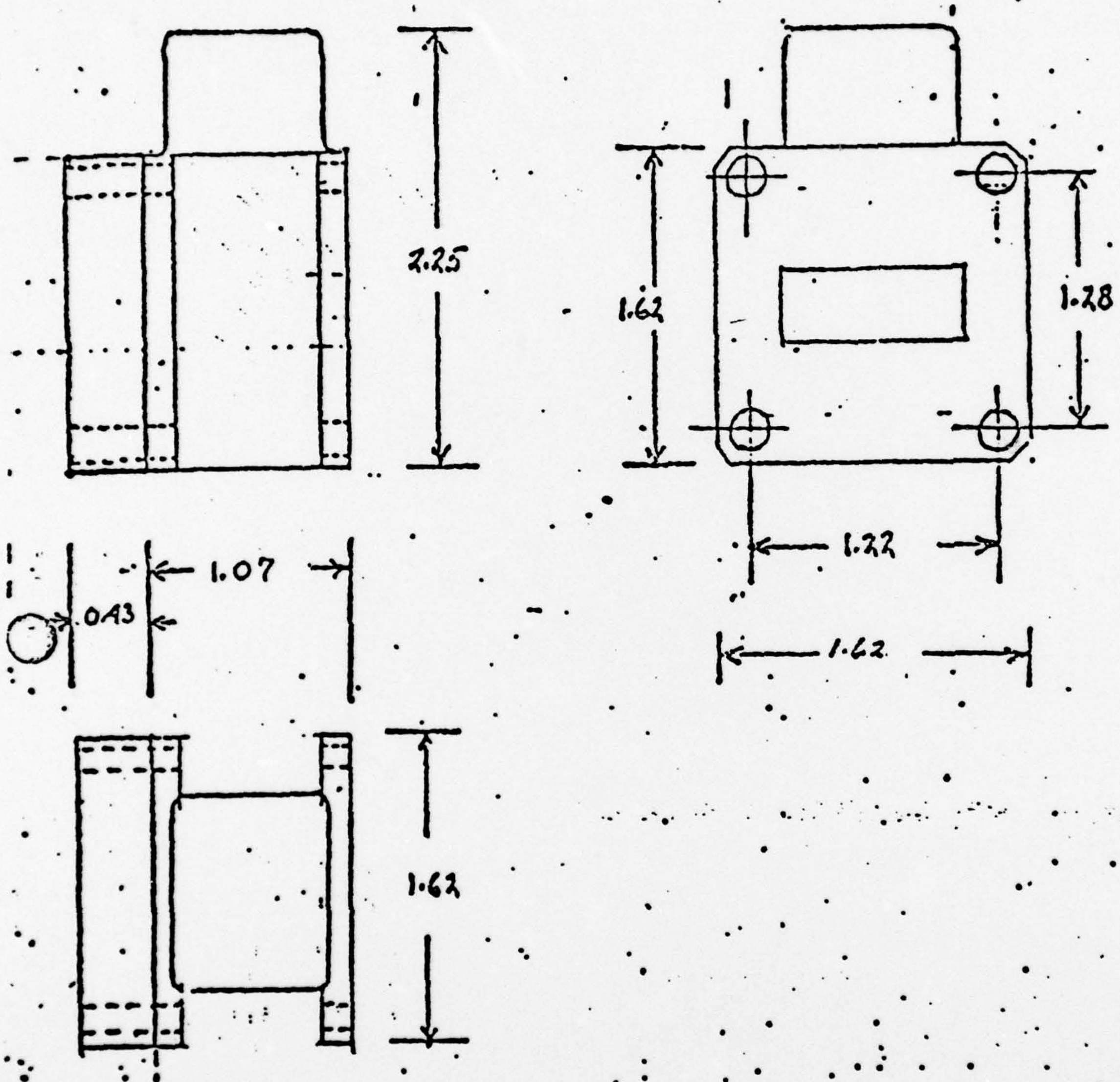
Measurement of parameters cited will follow the procedures outlined in QCI -1.

The bulk semiconductor limiter shall operate over the entire duration of the life test. The spike leakage (P_s), will be periodically monitored. Life test will be interrupted each 720 ± 20 hours intervals to permit testing of end of life test end points.

5. PREPARATION FOR DELIVERY

5.1 Packaging, Packing and Marking. - Packaging, packing and package rking shall be specified in the contract.

LINE DRAWING



Notes:

a) all dimensions in inches

b) all tolerances ± 0.01 unless otherwise specified

DISTRIBUTION LIST

	# CY
Department of Defense Deputy for Science and Tech. Ofc Assistant Secretary of the Army (R&D) Washington, DC 20310	1
Commander Picatinny Arsenal ATTN: SARPA-FR-S-P Dover, NJ 07801	1
Commander US Army Research Office ATTN: DRXRO-IP PO Box 12211 Research Triangle Pk, NC 27709	1
Commander US Navy Material Ind Res Office ATTN: Code 226 NAVMIRO Mr. Oscar Welskar Philadelphia, PA 19112	1
Director ARPA 1400 Wilson Blvd. Arlington, VA 22209	1
Commander Defense Documentation Center ATTN: TISIA-1 Cameron Station, Bldg. 5 Alexandria, VA 22314	12
Commander US Army Electronics Command ATTN: DRSEL-RD-EM-2 Fort Monmouth, NJ 07703	1
Director Electronic Components Lab ATTN: DRSEL-TL-IJ (G. Morris) Fort Monmouth, NJ 07703	1

	# CY
Director US Army Production Equipment Agcy ATTN: Manufacturing Tech Div. Rock Island Arsenal Rock Island, IL 61201	1
Commander Harry Diamond Laboratories ATTN: Mr. Horst Gerlach 2800 Powder Mill Rd. Adelphia, MD 20783	1
Commander US Army Material Readiness & Development Command ATTN: DRCPM-NXE-D (Dr. McClung) Nike X Project Office Redstone Arsenal, AL 35809	1
Director Electronic Components Lab ATTN: DRSEL-TL-IL (Mr. V. Higgins) Fort Monmouth, NJ 07703	1
Commander US Army Missile Command ATTN: AMSMI-IEVL (Mr. R. Buckelew) Building 4500 Redstone Arsenal, AL 35809	1
Office of Defense Research & Eng'g Communications and Delectronics Room 3D1037 Washington, DC 20330	1
Commander US Army Materiel Readiness & Development Command ATTN: DRCDE-D 5001 Eisenhower Ave. Alexandria, VA 22304	1

DISTRIBUTION LIST

	# CY
Commander US Naval Air Development Center ATTN: Library Johnsville Warminster, PA 18974	1
Chief Naval Ship Systems Command Dept of the Navy ATTN: Code 681A2b, Mr. L. Gumina Room 3329 Washington, DC 20330	1
Commander Dept of the Navy ELEX 05143A ATTN: A.H. Young Electronics System Command Washington, DC 20360	1
Commander US Naval Research Laboratory ATTN: G. Abraham 5205 Washington, DC 20390	1
Reliability Analysis Center ATTN: RADC-RBRAC Griffiss Air Force Base New York 13441	1
Commander Defense Electronics Supply Ctr Directorate of Engineering & Standardization ATTN: (DESC-ECS) Mr. N.A. Hauck Dayton, OH 45401	1
Commander Air Research & Development Command ATTN: RDTCT Andrews Air Force Base Washington, DC 20330	1
Commander Rome Air Development Center Griffiss Air Force Base ATTN: (EMERR) Mr. L. Gubbins Rome, NY 13440	1
Commander Rome Air Development Center Griffiss Air Force Base ATTN: (EMERR) Mr. Regis C. Hillow Rome, NY 13440	1
Commander Air Force Materials Lab ATTN: MATE (Mr. J. Wittebort) Electronics Branch Wright-Patterson Air Force Base Dayton, OH 45433	1
AFAL (AVTA) Electronic Technology Division ATTN: Mr. Robert D. Larson, Chief Advanced Electronics Devices Branch Wright Patterson Air Force Base Dayton, OH 45433	1
Advisory Group on Electron Devices 201 Varick St., 9th Floor New York, NY 10014	2
National Aeronautics & Space Admin George C. Marshall Space Flight Ctr ATTN: R-QUAL-FP (Mr. L.C. Hamiter) Huntsville, AL 35812	1
Commander US Army Electronics Command ATTN: DRSEL-PP-I-PI-1 Fort Monmouth, NJ 07703	2

DISTRIBUTION LIST

Addressee	# CY
NASA Manned Space Craft Center Reliability and Flight Safety Div ATTN: Mr. Lawrence Steinhardt Houston, TX	1
Scientific & Technical Info Facility ATTN: Acquisition Branch (S-AK/DL) PO Box 8757 Baltimore (Wash. Intl A/P, MD 21240	1
Avantek ATTN: Mr. Thielan 3001 Cooper Rd Santa Clara, CA 95051	1
AIL ATTN: Mr. Lou Cianciulli Commack Rd. Deer Park , LI, NY	1
American Electronics Laboratory Richardson Rd Comar, PA	1
Alpha Industries Inc. ATTN: Dr. W. K. Niblack 20 Sylvan Rd. Woburn, MA 01801	1
Bendix Corporation Semiconductor Div. ATTN: Mr. J. Ruskin South St. Holmdel, NJ 07733	1
Collins Radio Company Cedar Rapids Div. ATTN: Mr. W. Caldwell Cedar Rapids, IO 52406	1
General Micro-Electronics, Inc. 2920 San Ysidro Way Santa Clara, CA 95051	1
General Electric Company No. Concourse Bldg. Syracuse, NY 13212	1
General Motors Corp. Delco Radio Div. ATTN: Dr. E. Jaumot, Jr. PO Box 1104 Kokomo, IN 46901	1
General Instrument Corp. Semiconductor Products Group 600 W. John St. Hicksville, LI, NY 11802	1
Honeywell, Inc. Semiconductor Products 2747 Fourth Ave. Minneapolis, MN 55408	1
Micro Electronics Lab Hughes Aircraft Co 500 Superior Ave. Newport Beach, CA 92663	1
IBM Components Div. ATTN: Mr. Al Kran East Fishkill, Rt. 52 Hopewell Junction, NY 12533	1
KSC Semiconductor Corp. ATTN: Mr. S. Cudletz, Pres. KSC Way (Katrina Rd). Chelmsford, MA 01824	1
Arthur D. Little Acorn Park ATTN: Dr. H. Rudenberg 15/206 Cambridge, MA 02140	1

DISTRIBUTION LIST

	# CY
Raytheon Company Microwave Power Tube ATTN: R. E. Roberts Willow St. Waltham, MA 02154	1
Motorola, Inc. ATTN: Mr. J. LaRue 5005 East McDowell Rd. Phoenix, AZ 85008	1
Northrup Corporate Labs ATTN: Library 320-61 3401 West Broadway Hawthorne, CA 90250	1
Philco Ford Corporation Microelectronics Div. Church Rd. Lansdale, PA 19446	1
Raytheon Company Semiconductor Operation ATTN: Mr. S. Weisner 350 Ellis St. Mountain View, CA 94040	1
Dr. Robert H. Rediker MIT Bldg. 13-3050 Cambridge, MA 02139	1
Sprague Electric Co. ATTN: Mr. W.C. Donelan 87 Marshall St. North Adams, MA 01247	1
Solitron Devices, Inc. 256 Oak Tree Rd. Tappan, NY 10983	1

	# CY
Sanders Associates, Inc. ATTN: Microwave Dept. 95 Canal St. Nashua, NH	1
Texas Instruments Semiconductor Components Div. ATTN: Semiconductor Library PO Box 5012 Dallas, TX	1
Western Electric ATTN: Mr. R. Moore Maron & Vine Sts. Laureldale, PA	1
Varian Associates Solid State Div. ATTN: Mr. J. Collard 8 Salem Rd. Beverly, MA 01803	1
Commander Air Force Materiels Lab Wright Patterson AFB ATTN: AFML/STE (Ms. E. Tarrants) Dayton, OH 45433	1